UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,737	06/20/2003	Satoshi Ishikura	31638US4	7396

116 7590 08/11/2005

PEARNE & GORDON LLP
1801 EAST 9TH STREET
SUITE 1200
CLEVELAND, OH 44114-3108

EXAMINER	
WHITMORE, STACY	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,737	ISHIKURA, SATOSHI	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 5, 7–9, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Iida (US Patent 5,500,542).

2. As for claims 5, 7–9, and 15, Iida discloses the invention as claimed, including a method or designing, computer readable medium storing a program/ semiconductor device which is formed by (has means or) combining and disposing pre-registered/advance registered functional blocks, and determining a wiring pattern in accordance with a given logic specification, wherein at least one of the functional blocks has a logic circuit and a diode [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b]; and

The diode is composed of a first conduction type diffusion layer and a second conduction type well connected to an input terminal/ power source [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b],

The diode is connected to a potential-clamped input terminal of at least one of the functional blocks [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b; Further see col. 5, line 45 – col. 6, line 22; col. 8, lines 46-50]; and

wherein the diode is connected to a port between an output of the logic circuit and the input terminal of the functional block [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b; Further see col. 5, line 45 – col. 6,

line 22; col. 8, lines 46-50 – the diode is connected between a plurality of logic circuits and functional blocks and is therefore connected between a port of the output of at least one logic circuit and the input terminal of a functional block].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (US Patent 5,500,542) in view of Spaanenberg (US Patent 4,656,592).

4. As for claim 6, Iida discloses the invention substantially as claimed including the semiconductor device as rejected in claim 5 above.

Iida does not specifically disclose the logic circuit is a memory.
Spaanenberg shows a logic circuit being a memory [col. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Iida and Spaanenberg because utilizing a memory as a logic circuit would provide for storage in a microprocessor system thereby optimizing processing speed of the device [see Spaanenberg, col. 4, lines 45-55].

5. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (US Patent 5,500,542) in view of Katsube (US Patent 5,828,119).

6. As for claims 10-14, Iida discloses the invention substantially as claimed, including a method or designing, computer readable medium storing a program/ semiconductor device which is formed by combining and disposing pre-registered/advance registered functional blocks, and determining a wiring pattern in accordance with a given logic specification, wherein at least one of the functional blocks has a logic circuit and a diode [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b]; and
The diode is composed of a first conduction type diffusion layer and a second conduction type well connected to an input terminal/ power source [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b],
The diode is connected to a potential-clamped input terminal of at least one of the functional blocks [col. 1, lines 47-57, col. 14, lines 9-14; col. 15, line 45 – col. 16, line 45; figs. 5, 17, 20, 22, 23a – 25b].

Iida does not specifically disclose wherein a diode is connected to an input pin where the antenna ratio results exceed an allowed antenna ratio.

Katsube discloses connecting a diode when antenna ratio exceeds an allowed ratio [col. 9, line 49 – col. 10, line 38].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Iida and Katsube because connecting a diode to Iida's device when an antenna ratio exceeded an allowed ratio would improve Iida's system by preventing a design of a device where the device would be damaged to gate oxide resulting from excess voltage or current or buildup.

7. Applicant's arguments filed May 25, 2005 have been fully considered but they are not persuasive.
In the remarks, applicant argues in substance:

A: Iida nor Katsube disclose that the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Examiner respectfully disagrees:

As to A: Iida discloses that the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks [see as cited in the rejection of claim 1, and also col. 5, line 45 – col. 6, line 22; col. 8, lines 46-50; Iida at least discloses that the diode is connected to the input of the functional block and is inherently clamping the input terminal of the at least one functional block, and therefore reads on the claimed limitations]

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
August 6, 2005